Interfacing Synchronous DRAMs to Pentium Processors

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The steady increase in the bus frequencies of microprocessors necessitates the use of new memory technologies in order to keep up with these frequencies. Synchronous memory technologies in general, and Synchronous DRAMs in particular, offer advantages for these designs as they provide the required frequencies as well as a clean memory interface design due to their synchronous nature. We will discuss the design of a system based on the Intel Pentium microprocessor and SDRAMs. The memory interface between the Pentium and the SDRAMs is implemented using Gate Array Logic (GAL) devices.

The Processor

For the purposes of this design, the Pentium P54C-100/66 processor, operating at 100 MHz internal frequency and 66 MHz bus frequency was used. It is the bus frequency of the processor that is of importance in the design of a synchronous memory interface, as will be shown later in this paper.

The SDRAM Bank

A 2Mx64 SDRAM bank consisting of 8 pieces of 2Mx8 SDRAM is used in the design. The design can easily be modified to support a 2Mx32 SDRAM bank, since the Pentium supports a 32-bit memory interface by connecting the Pentium's A2 address to the appropriate memory address.

The Interface: Processor Signals

There are several Pentium signals that are relevant to the design of this memory interface. These signals and a description of their function per the Pentium Family User's Manual appear below.

1) ADS# output: The address status indicates that a new valid bus cycle is currently being driven by the Pentium processor.

2) Cache# output: For Pentium processor initiated cycles the cache pin indicates the internal cacheability of the cycle (if a read) and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the Pentium processor will not cache the data.

3) W/R# output: A logic "0" indicates a read.

4) BRDY# input: The burst ready input indicates that the external system has presented valid data on the data pins in response to a read or that the external has accepted the Pentium processor data in response to a write request.

5) NA# input: An active next address input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium processor will drive out a pending cycle two clocks after NA# is asserted.

6) BE0# - BE7# outputs: The byte enable pins are used to determine which bytes must be written to external memory, or which bytes are requested by the CPU for the current cycle.

7) A3 - A31 outputs: The address lines of processor along with the byte enable define the physical area of memory or I/O accessed.

The Interface: SDRAM Signals

As a general comment, the status of SDRAM signals are sampled at the rising edge of the clock on the device. For example, an assertion of RAS# is defined
as the signal being at logic "0" at the PLL rising edge of CLK.

1) RAS#: The Row Address Strobe.

2) CAS#: The Column Address Strobe.

3) WE#: The Write Enable signal. WE#, in conjunction with RAS# and CAS#, define the command being sampled.

4) B/S: The bank select signal defines to which bank the active, Read, Write or Precharge command is being supplied.

5) DQM: This signal, when sampled high, places the outputs in high-Z state in a Read cycle and acts as an output mask in a write cycle.

6) A[0..10] : The 11 address lines of the 2Mx8 SDRAM are multiplexed internally, similar to standard DRAMs. These addresses along with the bank select signal pinpoint the memory location to be read from or written to.

The Design

Refer to Figure 1, the top level block diagram of the design.

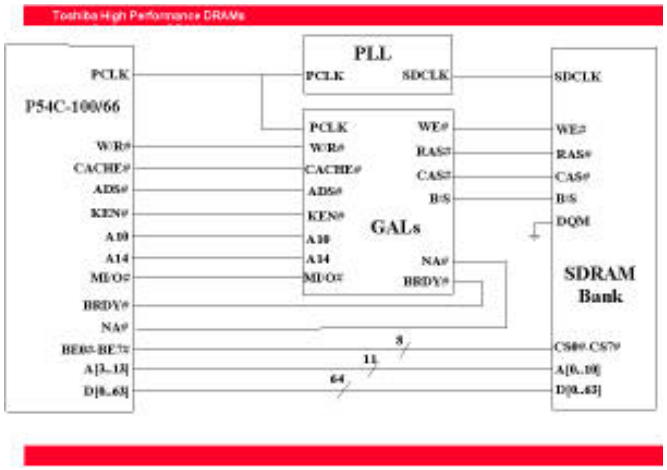

Figure 1. Pentium/SDRAM Interface: Top Level Block Diagram

1) PLL: Due to the speed at which the device is operated, a phase locked loop (PLL) circuit is used in the design. This can reside either on the motherboard or on the SDRAM memory module, if one exists. Note that the current JEDEC SDRAM dual in-line memory module (DIMM) specification recommends that a PLL be placed on the DIMM, between the processor clock and the SDRAM clocks.

2) GALs: For the purposes of this paper, the memory interface was designed using Gate Array Logic (GAL) devices. It is important to point out that this is not the only way of interfacing to SDRAMs. Other options could include off-the-shelf chip sets specifically designed to interface with SDRAMs, offered by various chip set manufacturers.

As mentioned above, the design uses a Pentium operating at a 66 MHz external bus, which translates to a 15.15 ns clock cycle time. The SDRAM clock frequency is 100 MHz which is equivalent to a 10ns clock cycle time. Therefore, the GAL devices used need to be 5ns or faster in order to meet these timing requirements.

3) Byte Enable: Each of the 8 Pentium byte enable signals is tied directly to the chip select signal of one of the SDRAM banks. In this way, each SDRAM will provide the byte corresponding to its location when selected.

4) Address: Pentium addresses A3-A13 are connected to SDRAM addresses A0-A10 directly.

5) Data: The 64 data lines on the SDRAM bus are directly connected to D0 - D63 of the Pentium. Alternatively, the designer may consider isolating the memory bus by using a very fast bi-directional buffer, such as a '244 device.

Implementation of the Design

Refer to Figure 2, which shows the details of the implementation of the interface.

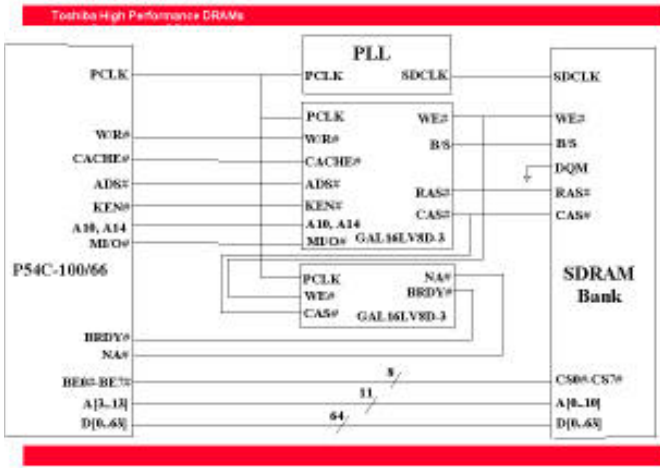

Figure 2. Pentium/SDRAM Interface

The interface was implemented using two pieces of the newly introduced 3.5ns 3.3V GAL devices from Lattice Semiconductor.

The specific part number of the device is GAL16LV8D-3LJ. This device is a registered GAL with 16 inputs and 8 outputs. Any one of the registered outputs may be bypassed. The first GAL is configured as a 16R6 and is used to generate the RAS# and CAS# signal to the memory bank. The second GAL is also configured as a 16R6 and is used to generate NA# and BRDY#.

As for the PLL, a Motorola MC952 PLL is used. This device is currently used in some SDRAM modules in the industry.

Read Cycle Example

Figure 3 shows an example of an interleaved bank read cycle.

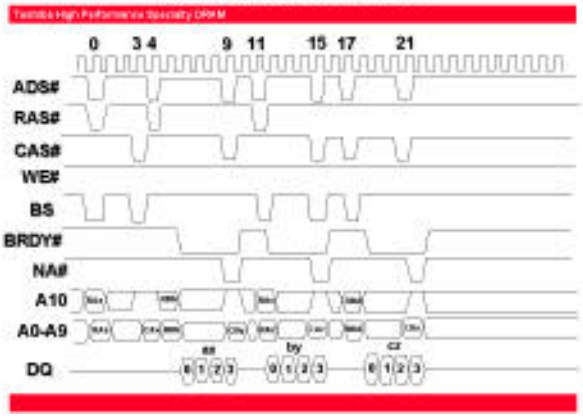

Figure 3. Interleaved Bank Read

For the purposes of this paper, the CAS latency, i.e. the number of clocks from the time the CAS# signal is asserted low until the time that the first byte of data is read, is set to 3 cycles, which is equivalent to 30ns. Also, the burst length is set to 4.

A detailed description of the read cycle as depicted in Figure 3 follows.

The Pentium processor initiates a read cycle by asserting the address status signal (ADS#) in the first clock. The clock in which ADS# is asserted is by definition the first clock in the bus cycle, defined to be CLK0 in this paper. The ADS# output indicates that a valid bus cycle definition and address is available on the bus cycle definition pins and the address bus. The CACHE# output is deasserted (high) to indicate the cycle will be a single transfer cycle.

CLK0: A BankActive command is issued to bank A by setting RAS# and BS low. BS is set low as the first read is from bank A. Row address “a” in bank is presented to the memory.

CLK3: A Read and AutoPrecharge command is issued to bank A by holding the A10 signal high.

CLK6: The SDRAM has a RAS latency of 3. Therefore, 3 clocks after the assertion of CAS# (CLK6) the first of data is read from the device. Since a burst length of 4 is assumed, the second, third and fourth piece of data appear on clocks 7, 8 and 9 respectively.

Note that the implementation of burst cycles on the Pentium processor is via the BRDY# pin. Correspondingly, BRDY# is asserted during clocks 6, 7, 8 and 9. Also, the next address (NA#) input to the processor indicates that the external memory system is ready to accept a new bus cycle, although all data transfers for the current cycle have not yet completed.

The next read in this example is a 4 bit burst from the bank B. In the case of a burst of 4, it is not possible to get a contiguous stream of data from the device. (Note: It is possible to get contiguous data from the device with a burst length of 8. Choosing a burst length of 8, however, will add a third GAL to the design). It is important to see why reading contiguous data in the case of a burst length of 4 is not possible. This is explained below by tracing the timings in Figure 3 in detail.

CLK4: The read from bank B is initiated on CLK4 by asserting ADS# and RAS# and providing the appropriate row address. It is important to note that the precharge command timing cannot occur before one burst length (i.e. 4 cycles) after the column address for the previous read command to bank A is provided. Therefore the precharge occurs on clock 7. In addition, the design must satisfy the Precharge to Active command timing, tRP, on the SDRAM. This is specified to be 36ns, or 4 cycles. tRP ends on CLK11, therefore the first clock on which data can be read from the bank B is CLK12.

Appropriately, a Read with AutoPrecharge command to bank B is issued on CLK9 by asserting ADS# and RAS#.

The third read in the example is again from bank A. Following a line of reasoning similar to the one above, the first byte of data is read on CLK18, therefore the Read with AutoPrecharge command to bank A is issued on CLK15.

Write Cycle Example

Figure 4 shows an example of an interleaved bank write cycle.

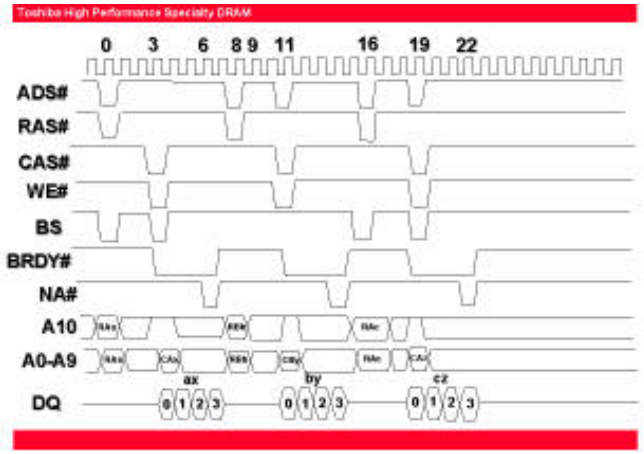

Figure 4. Interleaved Bank Write

A detailed description of the write cycle as depicted in Figure 4 follows.

As in the case of a read cycle, the Pentium processor initiates a write cycle by asserting ADS# on CLK0.

CLK0: RAS# is asserted to initiate the cycle. BS is set low as the first write is to bank A. Row address “a” in bank A is presented to the memory.

CLK3: CAS# and WE# are asserted, in conjunction with BS=low and the column address “x” in bank A is presented to the memory. The first byte of data is read in this cycle. Since a burst length of 4 is assumed, subsequent bytes of data appear on clocks 4, 5 and 6. Correspondingly, BRDY# is asserted on clocks 3, 4, 5 and 6.

CLK6: NA# is asserted to indicate to the processor the readiness of the memory to accept a new bus cycle.

CLK8: The second write operation to the memory, which is a write to bank B, is initiated on CLK8 by asserting ADS# and RAS#, and presenting the valid row address “b”.

CLK11: ADS#, CAS# and WE# are asserted, A10 is set high, and column address “y” is presented to define a Write with AutoPrecharge cycle. The data to be written to bank B of the memory is presented on clocks 11, 12, 13 and 14 respectively. BRDY# and NA# are asserted appropriately.

CLK16: The third write cycle in the example is a write to bank A. Having satisfied the burst length and tRP timings as discussed in the case of a read, the third cycle is initiated on CLK16 by asserting ADS# and RAS#, holding BS low and presenting the valid row address.

CLK19: A Write with AutoPrecharge command is issued on CLK19. Therefore, the data to be written is presented on clocks 19, 20, 21 and 22.

Finally, BRDY# is asserted on clocks 19, 20, 21 and 22, and NA# is asserted on clock 22 to indicate that the memory bank is ready for the next transaction.

Other signals

The DQM signal is connected to ground, since read data is not being tristated and write data is not being masked in this case.

Appendix: ABEL files for the design

```
module psdram1
title 'pentium sdram interface 1
                                u1    device  'P16R8';
Pclk, !WR, !Cache, !ADS, !KEN   pin   1, 2, 3, 5, 6;
A10, A14                        pin   7, 8;
!WE                             pin   19;
BS                              pin   12;
!RAS                            pin   13;
!CAS                            pin   14;
Q2, Q3, Q4                      pin   16, 17, 18;
MIO                             pin   4

equations

BS = A14 ;
!WE = !ADS & MIO & !Cache & KEN & WR ;
!RAS := !ADS & MIO & !Cache ;
!Q2 := !RAS ;
!Q3 := !Q2 ;
!Q4 := !Q3 ;
!CAS := (!WE & !Q2) # (WE & !Q4) ;

end psdram1
```

```
module psdram2
title 'pentium sdram interface 2

                        u2    device  'P16R8' ;
      Pclk, !WE, !CAS   pin   1, 2, 3 ;
          !BRDY, !NA    pin   12, 13 ;
Q4, Q5, Q6, Q7, Q8      pin   14, 15, 16, 17, 18 ;

equations

!NA := (!WE & !Q6) # (WE & !Q9) ;
!BRDY := (WE & !Q6 & !Q7 & !Q8 & !Q9) # ( !WE & !CAS & !Q4
& !Q5 & !Q6) ;
!Q4 := !CAS ;
!Q5 := !Q6 ;
!Q6 := !Q5 ;
!Q7 := !Q6 ;
!Q8 := !Q7 ;
!Q9 := !Q8 ;

end psdram2
```

REFERENCES

1) Intel Pentium Family User's Manual, Volume 1: Data Book
2) Toshiba America Electronic Components 2Mx8 SDRAM datasheet, 1995
3) Lattice Semiconductor GAL16LV8D device datasheet

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